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REMARKS

Claims 1-32, as amended, remain in this application. In view of the foregoing amendments, and remarks that follow, Applicant requests favorable considerable and timely indication of allowance.

The Examiner has acknowledged that claims 3-8, 10-13, 16-21 and 24-32 are directed to patentable subject matter. The Examiner has objected to these claims, however, as being dependant from rejected base claims indicating that allowance will be forthcoming if these claims are rewritten in independent form. Notwithstanding, Applicant has elected not to amend these claims at this time because Applicant believes the Examiner's rejection of the base claims is improper.

Claims 1, 2, 9, 14, 15, 22 and 23 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Alidina (US 6,064,714). These rejections are respectfully traversed.

Alidina discloses, in the background portion of the patent, a circuit capable of shifting data by a number of bit positions specified by a shift value in an auxiliary register. The shifting circuit include n stages of 3:1 multiplexers, where n is the number of bits of the shift value. Each 3:1 multiplexer implements one of three shifting operations depending on the shift value (i.e., a left shift, a right shift, or no shift). In particular, each 3:1 multiplexer implements either a no shift operation or a full shift operation in response to one bit of the shifting value. If the 3:1 multiplexer implements a full shift, a left/right shift control is used to shift the data right or left by the full amount. The problem with this approach is that the 3:1 multiplexers tend to be large, slow and power consuming.

Applicant discloses a novel and unobvious shifter circuit that reduces the shifting operations of each stage to two. By way of example, a multiple stage shifter circuit may be implemented with a first stage capable of performing a no shift operation or a right shift operation, and second and third stages each capable of performing right or left shift operations. With this approach, the 3:1 multiplexers used in Alidina may be replaced by smaller, faster, and lower power 2:1 multiplexers, or any other device capable of performing two shifting operations.

The Examiner takes the position that claims to a shifter element configured to perform "one of two shifting operations" reads on Alidina's multiplexer which performs three shifting operations. According to the Patent Office, "if three shifting operations are possible, then it

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follows that two shifting operations must be possible." Although Applicant does not necessarily agree with the Examiner's position, to advance the prosecution of this case, the claims have been amended to recite a shifter element configured to perform "one of only two possible shifting operations." (emphasis added). In other words, the shifting element is capable of performing only two shifting operations, and a shift control bit is used to select one of the two possible shifting operations. This amendment is being made to better clarify the claims, and is not a narrowing amendment made for reasons of patentability. Accordingly, Applicant respectfully requests that the pending rejections of the claims be withdrawn.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested. Should any issues remain which the Examiner believes could be resolved in a telephone interview, the Examiner is requested to telephone Applicant's undersigned attorney.

If there are any fees due in connection with the filing of this response, please charge such fees to our Deposit Account No. 17-0026. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for, such an extension is requested and the fee should also be charged to our Deposit Account. A duplicate copy of this page is enclosed.

Respectfully submitted,

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